REMARKS

The claims are claims 1, 3, 9, 10, 12 and 18 to 20.

The application has been amended to include references to new Figures 5 and 6.

New Figures 5 and 6 are added according to the attached drawing sheet. These new Figures illustrate the difference in transistor width between first and second cells.

Claims 1, 3, 10, 12, 19 and 20 are amended. Claim 1 has been amended to incorporate subject matter previously recited in claim 3 and canceled claim 7. Claim 3 has been amended to cancel the limitation incorporated into claim 1. Claim 10 has been amended to recite subject matter previously recited in canceled claim 11 and claim 12. Claim 12 has been amended to cancel the limitation incorporated into claim 10. Claims 19 and 20 have been amended similarly to corresponding claims 1 and 10.

The Examiner objected to the drawings under 37 CFR 1.83(a) as not illustrating the limitations recited in claims 3, 7, 8, 12, 16 and 17.

New Figures 5 and 6 are added to illustrate the differing transistor widths previously recited in claims 7 and 16. The Applicants respectfully submit that all other limitations of original claims 3, 7, 8, 12, 16 and 17 are either illustrated in the drawings, are not susceptible to illustration or have been canceled. The Table below points out where each element is illustrated.

In the Drawings

Please add Figures 5 and 6 per attached sheet.

Claim	Limitation	Reference
3	adder	114
	saturation detector	116
	input register	106
	result register	118
	critical path	not illustrated
7	width	511, 521 512, 521
8	time	canceled
12	adder	314
	saturation detector	316
	input register	306
	result register	318
	critical path	not illustrated
16	width	
17	time	canceled

The Applicants respectfully submit that the critical paths recited in claims 1, 10, 19 and 20 are not susceptible to illustration. The application states in paragraph [0004] at page 2, lines 11 to 20 that the circuit may include more than ten thousand critical paths. The application further states in paragraph [0004] at page 2, lines 26 to 28 that a Wallace tree cell " may be involved in greater than four thousand critical paths, greater than six thousand critical paths, or greater than eight thousand critical paths." Figure 4 includes a legend that indicates that some cells may have: more than 8001 critical paths; 6001 to 8000 critical paths; 4001 to 6000 critical paths; 2001 to 4000 critical paths; and 1 to 2000 critical paths. It is not feasible to illustrate such a large number of critical paths. The application includes text at paragraph [0004] page 2, lines 11 to 20 and paragraph [0031] page 12, lines 3 to 14 that clearly define critical paths.

Accordingly, the Applicants respectfully submit that the draws are proper.

Claims 1, 2, 4 to 6, 9 to 11, 13 to 15, and 18 to 20 were rejected under 35 U.S.C. 102(e) as anticipated by Hansen et al. U.S. Patent Application Publication No. US 2003/0110197A1.

Claims 1, 10, 19 and 20 recite subject matter not anticipated by Hansen et al. Claims 1, 10, 19 and 20 each recite critical paths and that first cells include such critical paths and second cells do not. Claims 1 and 19 each recite that "a critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time, wherein said predetermined amount of time is less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core." Claims 10 and 20 include similar recitations relative to a parallel multiplier core. Hansen et al includes not teaching regarding such critical paths. Accordingly, claims 1, 10, 19 and 20 are allowable over Hansen et al.

Claims 1, 10, 19 and 20 recite further subject matter not anticipated by Hansen et al. Claims 1 and 10 recite first and second cells that are " structurally the same." Claims 1 and 10 recite that "a width of at least one of said first plurality of transistors" forming the first cells "is greater than a width of a corresponding one of said second plurality of transistors" forming the second cells. Claims 19 and 20 recite that the first Wallace tree cells are structurally the same as the second Wallace tree cells and that the first Booth decoder cells are structurally the same as the second Booth decoder cells. Claims 19 and 20 each recite that the first plurality of transistors of the first cells are a first width and that the corresponding second plurality of

transistors of the second cells are a second smaller width. Thus claims 1, 10, 19 and 20 each recite cells that are structurally the same with differing transistor widths. Hansen et al includes no teaching regarding the width of a transistor. Therefore Hansen cannot anticipate this limitation of claims 1 and 10.

Claims 9 and 18 recite subject matter not anticipated by Hansen et al. Claims 9 and 18 recite " said at least one second cell is a most significant bit or a least significant bit and said at least one first cell is not a most significant bit or a least significant bit." Respective base claims 1 and 10 recite that first cells include a critical path and second cells do not. Hansen et al includes no teaching regarding critical paths and no teaching that most significant bits or least significant bits are do not a critical path. Accordingly, claims 9 and 18 are allowable over Hansen et al.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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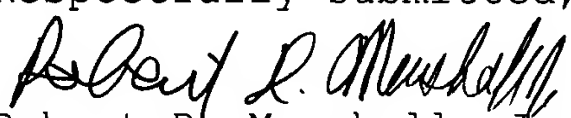
Respectfully submitted,



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